



Hogan & Hartson 81863.0022
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Actuator, Its Manufacturing Method...
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4 Drawing Sheets; Sheet 1 of 4

FIG. 1(a)

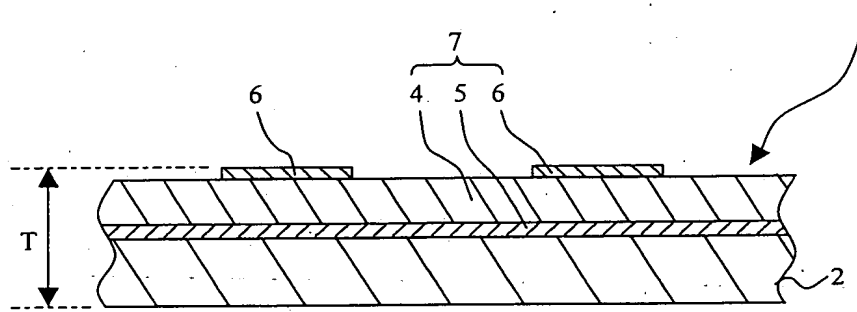
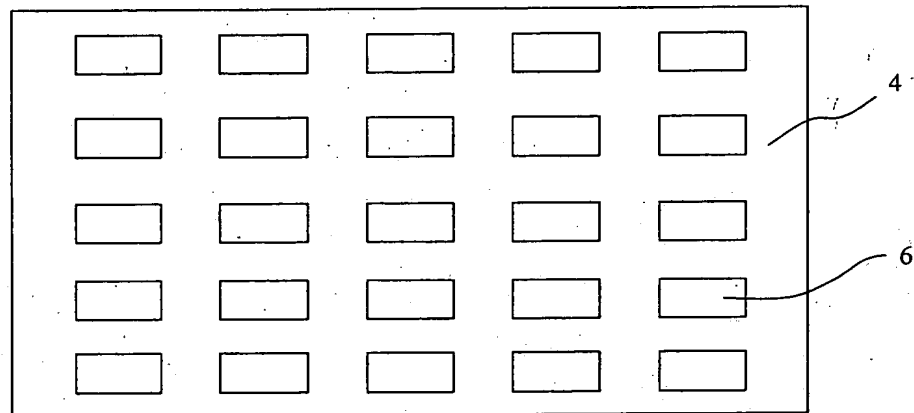


FIG. 1(b)



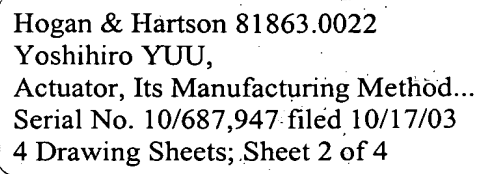


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 11 with a layer 12. A patterned layer 13 is formed on the substrate, with a top layer 14. A bracket 17 groups layers 14, 15, and 16. Other labels include 16, 18, 13a, and 13b.



FIG. 3(a)

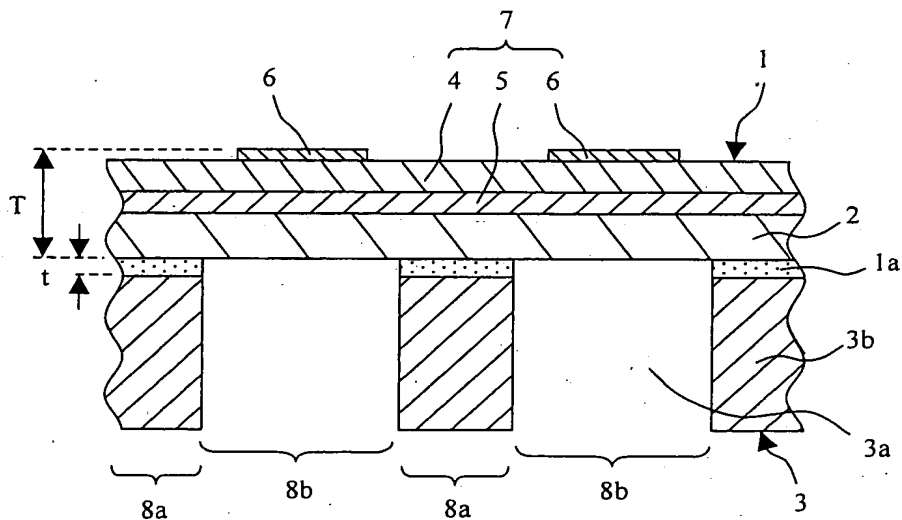
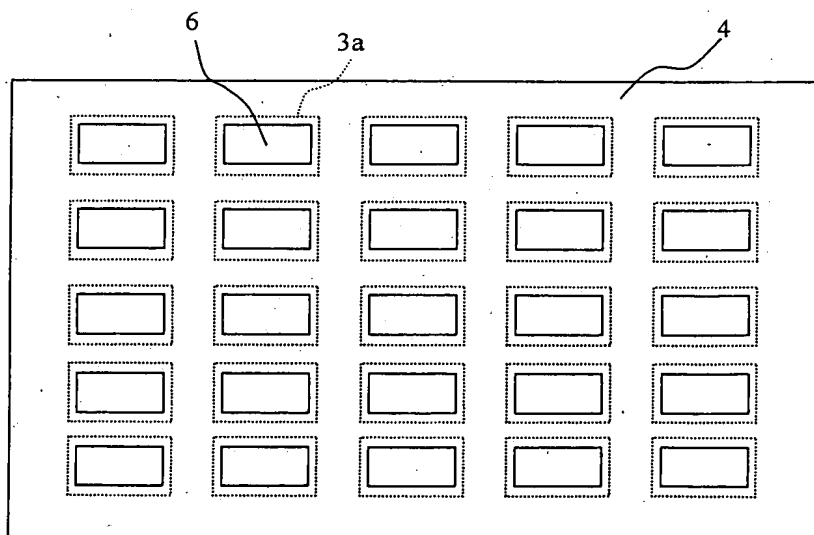
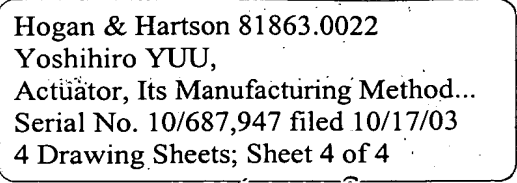


FIG. 3(b)





A cross-sectional view of a semiconductor device. It shows a substrate 23 with a central channel region 23a and side regions 23b. Two gate electrodes 21 are positioned on top of the substrate, separated by a distance d_x . Each gate electrode 21 consists of a top layer 27 and a bottom layer 21a. The bottom layer 21a is divided into regions 24, 25, and 26. The top layer 27 is divided into regions 24N, 25N, and 26N. The vertical distance between the top and bottom layers is labeled d_y . A gate contact 28 is shown on the side of the substrate 23, connected to the bottom layer 21a.